ITCE 321	Date:10/3/2013
Section:2	Quiz No. 1
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Q1- Explain the difference between the 3 (M-M), 2(M-M) , 1 (R-M), and 0- address machines in term of memory access, code size and execution speed:

Use the following numbers as comparison criteria (1, 2, 3, and 4) where 1 is lowest, 4 is highest.

Machine	Memory access	Code size	Execution speed
3-address (M-M)	3 times (4)	1+3x3=10 byte (4)	10 to fitch and 9 to Execute = 19 byte (1)
2-address (M-M)	2 times (3)	1+3x2=7 byte (3)	7 to fitch and 6 to Execute = 13 byte (2)
1-address (R-M)	1 time (2)	1+3=4 byte (2)	4 to fitch and 3 to Execute = 7 byte (3)
0-address	1 time or none (1)	1 or 4 byte (1)	4 to fitch and 3 to execute = 7 byte or 1 (4)

Q2- Consider the following expression:

$$A = [(N - Z/N) \ / \ (N*M - Z) * Y]$$

i. Evaluate the following expression using:
   1. Stack machine
   2. Load/Store machine

Assuming that A, N, M, Y, Z are stored in memory.

Stack machine	Load/Store machine

Push N
Push Z
Push N
Div
Sub
Push N
Push M
Mul
Push Z
Sub
~~Add~~
Push Y
Mul
~~Sub~~ ← Div
Pop A
	La r1, N
	La r2, Z
	div r3, r2, r1
	~~Sub r~~
	Sub r3, r1, r3
	La r4, M
	Mul r5, r1, r4
	~~La r4~~
	Sub r5, r5, r2
	La r4, Y
	mul r5, r5, r4
	Div r3, r3, r5
	St r3, A

$r_3 = \frac{Z}{N}$

$r_3 = N - \frac{Z}{N}$

$r_5 = N * M$

$r_5 = N*M - Z$

$r_5 = (N*M - Z)*Y$

$N*M - Z$

$N - \frac{Z}{N}$

$(N*M - Z)*Y$

$N - \frac{Z}{N}$

ii. Assuming that the machine has 128 registers, 65 instructions and memory space equal 3 Gbytes. Calculate:

Opcode specifier = 8 bits Memory specifier = 3×2^{30} Register specifier = 7 bits for each register

2^7 128
2^6 64
2^5 32
2^4 16
2^3 8
2^2 4

iii. The instructions code size (in bits) that are needed to execute the expressions:

Code size (Stack machine) = [8 | 24] = 24+8 = 32 bits (opcode | OP1)

or [8] = 8 bits (opcode)

Code size (accumulator machine) =

[8 | 24] = 32 bits (opcode | OP1)

1.5

Q3- For the following instructions which instruction is correct and which is not correct, Correct the incorrect one:

Instruction	correct	Correction if nay
brlnv r6, r4	x	brnv r4
brmi r1,r4, r7	x	brmi r1, r4, r7
brl r6	x	br r6
brlpl r3,r2	x	brpl r3, r2
brl r7, r12, r2	x	br r12 or brlpl r7, r12, r2 / brlmi r7, r12, r2

PC → r7
r2 condition r12 → PC

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Q4- What is the meaning of each of the following instructions? Encode each of them and show the corresponding condition for each instruction. (6 marks)

1- brmi r18, r24, r2

PC → R[18]
if R[2] < 0
R[24] → PC

| if the value in R[2] is minus branch to address in R[24]

2- br r4

R[4] → PC | Branch always to Address in R[4]

3- brl r6, r4

PC → R[6]
R[4] → PC

| Branch always to address in R[4] but store ~~value~~ what in PC in R[6] first